CLAIMS

What is claimed is:

1. An integrated circuit structure comprising:

first-type transistors and second-type transistors formed on the same substrate,

wherein said first-type transistors and said second-type transistors comprise:

gate conductors over channel regions in said substrate;

sidewall spacers adjacent said gate conductors; and

source and drain extensions on opposite sides of said channel regions,

wherein said sidewall spacers are larger in said first-type transistors than in said second-type transistors.

2. The integrated circuit structure in claim 1, wherein said source and drain extensions are spaced further from said channel regions in said first-type transistors than in said second-type transistors.

3. The integrated circuit structure in claim 1, further comprising silicide regions between portions of said sidewall spacers and said substrate, wherein said silicide regions are larger in said first-type transistors than in said second-type transistors.

4. The integrated circuit structure in claim 1, wherein said sidewall spacers include oxide liners, and

wherein said oxide liners are thicker in said first-type transistors than in said second-type transistors.

5. The integrated circuit structure in claim 1, wherein said sidewall spacers comprise multiple-layer sidewall spacers, and

wherein said sidewall spacers in said first-type transistors have more sidewall spacer layers than in said second-type transistors.

6. The integrated circuit structure in claim 1, wherein said first-type transistors have different performance characteristics than said second-type transistors.

7. The integrated circuit structure in claim 1, wherein source and drain extensions in said first-type transistors are made of a different material than in said second-type transistors.

8. An integrated circuit structure comprising:

P-type field effect transistors (PFETs) and N-type field effect transistors (NFETs) formed on the same substrate,

wherein said PFETs and said NFETs comprise:

gate conductors over channel regions in said substrate;

sidewall spacers adjacent said gate conductors; and

source and drain extensions on opposite sides of said channel regions,

wherein said sidewall spacers are larger in said PFETs than in said NFETs.

9. The integrated circuit structure in claim 8, wherein said source and drain extensions are spaced further from said channel regions in said PFETs than in said NFETs.

10. The integrated circuit structure in claim 8, further comprising silicide regions between portions of said sidewall spacers and said substrate, wherein said silicide regions are larger in said PFETs than in said NFETs.

11. The integrated circuit structure in claim 8, wherein said sidewall spacers include oxide liners, and

wherein said oxide liners are thicker in said PFETs than in said NFETs.

12. The integrated circuit structure in claim 8, wherein said sidewall spacers comprise multiple-layer sidewall spacers, and

wherein said sidewall spacers in said PFETs have more sidewall spacer layers than in said NFETs.

13. The integrated circuit structure in claim 8, wherein said PFETs have different performance characteristics than said NFETs.

14. The integrated circuit structure in claim 8, wherein source and drain extensions in said PFETs are made of a different material than in said NFETs.

15. A method of forming an integrated circuit structure having first-type transistors and second-type transistors on the same substrate, said method comprising:

forming gate conductors above channel regions in said substrate;

forming sidewall spacers adjacent said gate conductors, wherein said sidewall spacers are larger in said first-type transistors than in said second-type transistors; and

forming source and drain extensions in said substrate.

16. The method in claim 15, wherein said process of forming said source and drain extensions forms said source and drain extensions further from said channel regions in said first-type transistors than in said second-type transistors.

17. The method in claim 15, wherein said process of forming said source and drain extensions comprises implanting said source and drain extensions, wherein said sidewall spacers align said source and drain extensions during said implanting process.

18. The method in claim 15, wherein said process of forming said sidewall spacers includes forming an oxide liner, wherein said oxide liner is thicker in said first-type transistors than in said second-type transistors.

19. The method in claim 18, wherein oxide liners for said first-type transistors are formed in a different processing step than oxide liners for said second-type transistors.

20. The method in claim 17, wherein said process of forming said sidewall spacers includes forming a multiple-layer sidewall spacers, wherein said sidewall spacers in said first-type transistors have more sidewall spacer layers than in said second-type transistors.

21. The method in claim 15, further comprising forming silicide regions between portions of said sidewall spacers and said substrate, wherein said silicide regions are larger in said first-type transistors than in said second-type transistors.

22. A method of forming an integrated circuit structure having P-type field effect transistors (PFETs) and N-type field effect transistors (NFETs) transistors on the same substrate, said method comprising:

forming gate conductors above channel regions in said substrate;

forming sidewall spacers adjacent said gate conductors, wherein said sidewall spacers are larger in said PFETs than in said NFETs; and

forming source and drain extensions in said substrate.

23. The method in claim 22, wherein said process of forming said source and drain extensions forms said source and drain extensions further from said channel regions in said PFETs than in said NFETs.

24. The method in claim 22, wherein said process of forming said source and drain extensions comprises implanting said source and drain extensions, wherein said sidewall spacers align said source and drain extensions during said implanting process.

25. The method in claim 22, wherein said process of forming said sidewall spacers includes forming an oxide liner, wherein said oxide liner is thicker in said PFETs than in said NFETs.

26. The method in claim 18, wherein oxide liners for said PFETs are formed in a different processing step than oxide liners for said NFETs.

27. The method in claim 17, wherein said process of forming said sidewall spacers includes forming a multiple-layer sidewall spacers, wherein said sidewall spacers in said PFETs have more sidewall spacer layers than in said NFETs.

28. The method in claim 22, further comprising forming silicide regions between portions of said sidewall spacers and said substrate, wherein said silicide regions are larger in said PFETs than in said NFETs.